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PATENT & TRADEMARK OFFICE

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ATTENTION: BOX AFTER FINAL
RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE REQUESTED
EXAMINING GROUP 2814
Customer No. 22,852
Attorney Docket No. 08245.0027

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#9 Amdt
M. Bonner
N/E
9/6/03

In re Application of:

Jun Dong KIM et al.

Serial No.: 09/892,878

Filed: June 28, 2001

For: METHOD FOR FORMING GATE ELECTRODES IN A SEMICONDUCTOR DEVICE USING FORMED FINE PATTERNS

Group Art Unit: 2814

Examiner: S. Rao

enter
Marsha
5/13/03

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TECHNOLOGY CENTER 2800

Commissioner for Patents and Trademarks
Washington, DC 20231

Sir:

AMENDMENT AFTER-FINAL AND REQUEST FOR RECONSIDERATION

In response to the Final Office Action dated December 3, 2002, and pursuant to 37 C.F.R. § 1.116, Applicants propose that this application be amended as follows:

IN THE CLAIMS:

Please amend claims 6 and 8 as indicated in the attached Appendix and as presented below:

6. (Amended) A method for forming fine patterns of a semiconductor device, the method comprising:

forming a patterning layer over a semiconductor wafer;

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